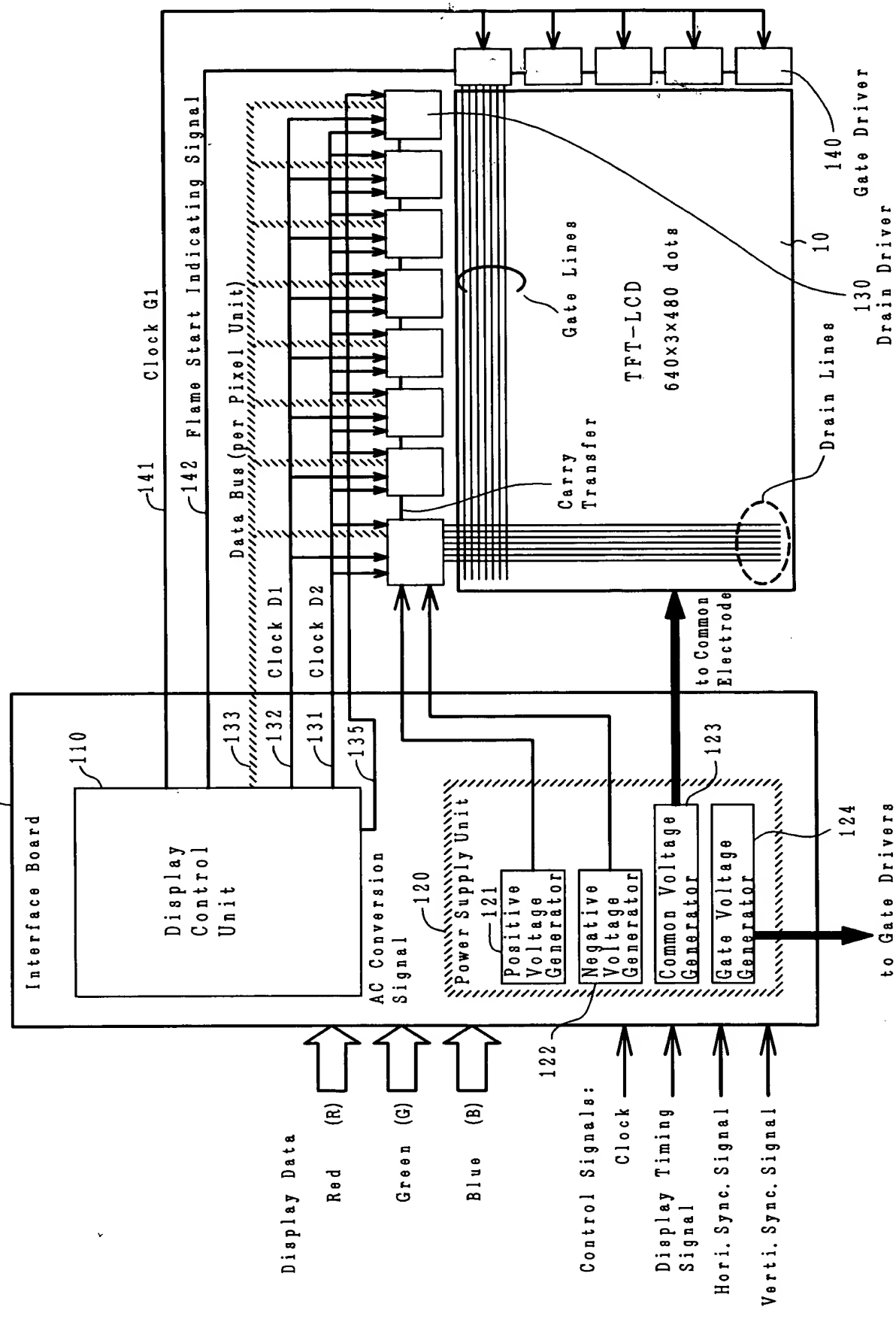


SECRET" SET428T60

FIG. 1



The diagram illustrates a pixel circuit within a grid defined by dashed lines. The horizontal axis is labeled 'D' at the top left, and the vertical axis is labeled 'G' on the left side. A common source line is labeled 'COM'. The gate line is labeled 'A R'. The data line is labeled 'V COM'. The circuit includes transistors TFT1 and TFT2, capacitors CLC and CSTG, and resistors ITO1 and ITO2. The circuit is organized into columns corresponding to different colors: G (Green), B (Blue), and R (Red). Each column contains a series of transistors and capacitors connected to the gate and data lines.

FIG. 7

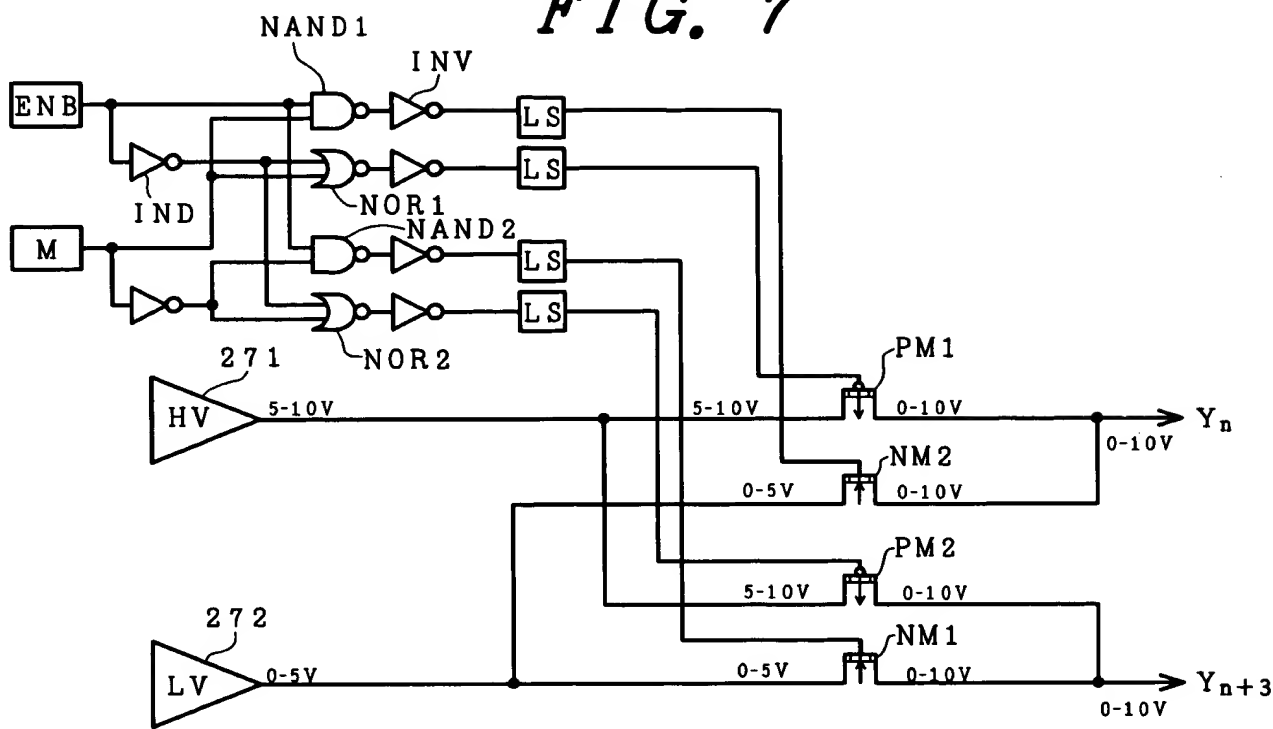
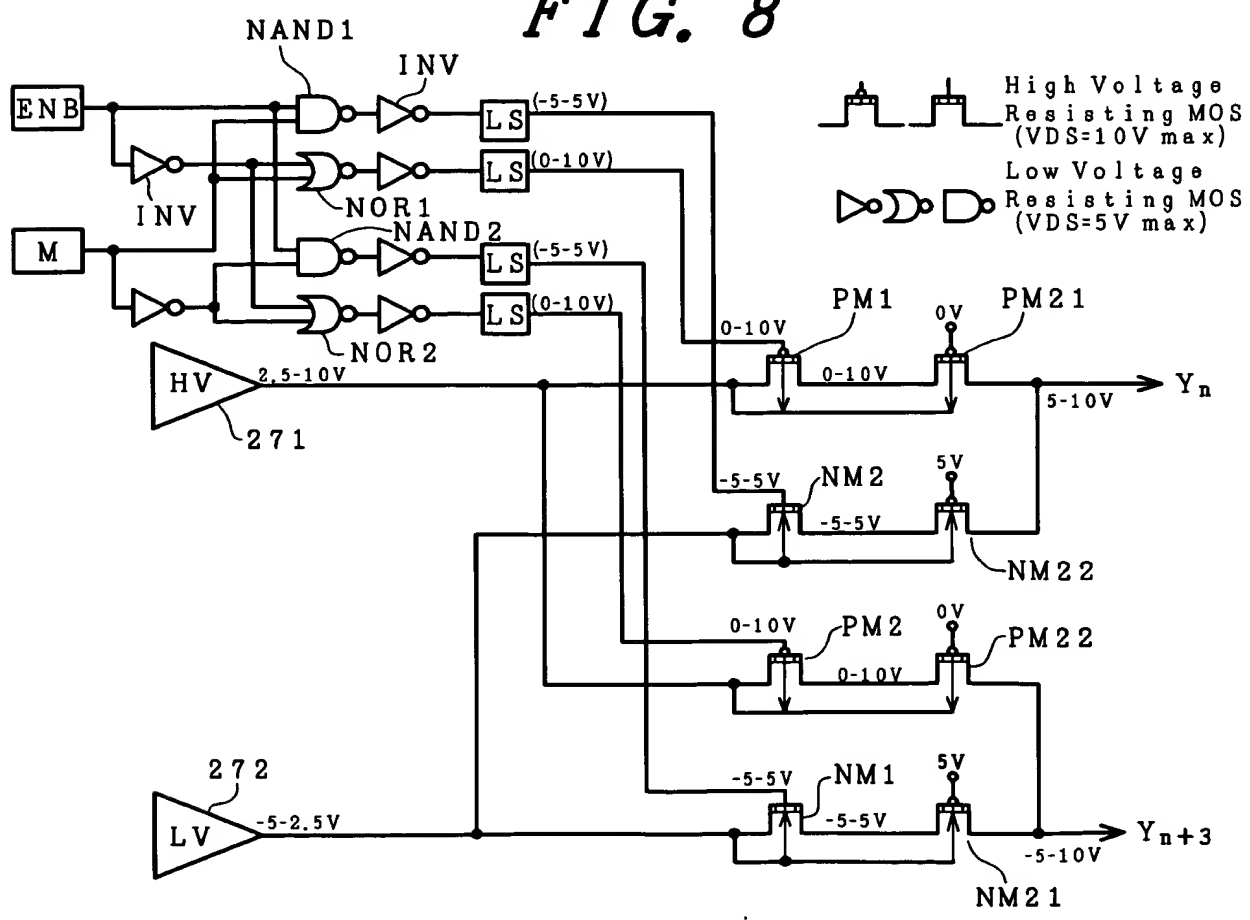
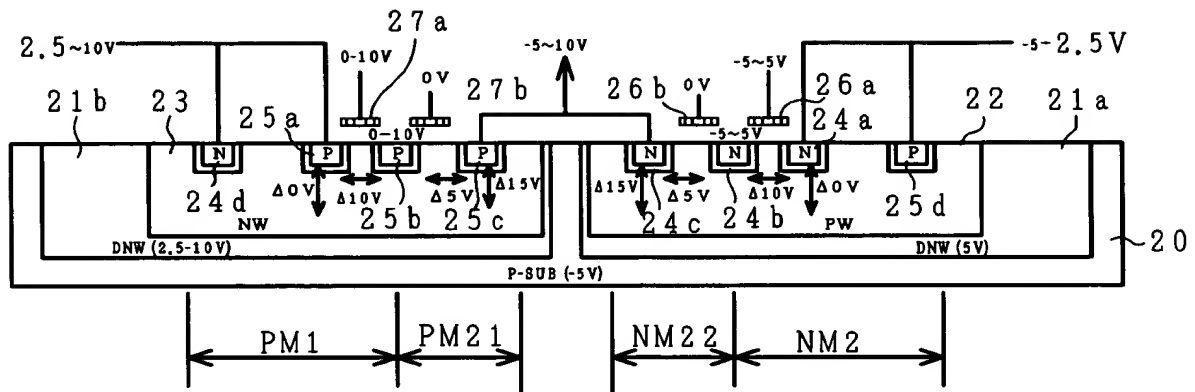


FIG. 8



09182445 103099

FIG. 9



850201 " 0243160

FIG. 10A

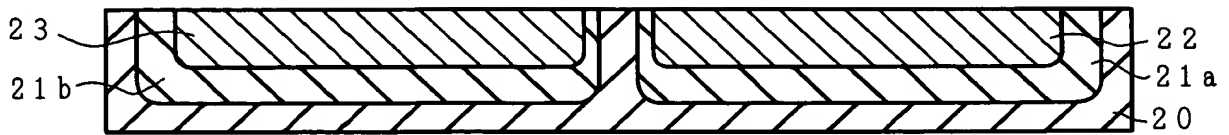


FIG. 10B

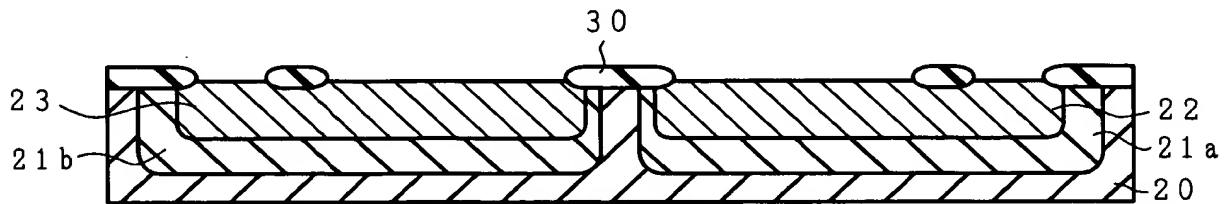


FIG. 10C

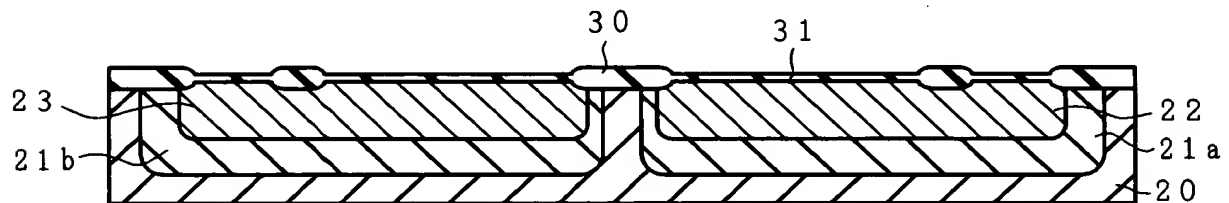


FIG. 10D

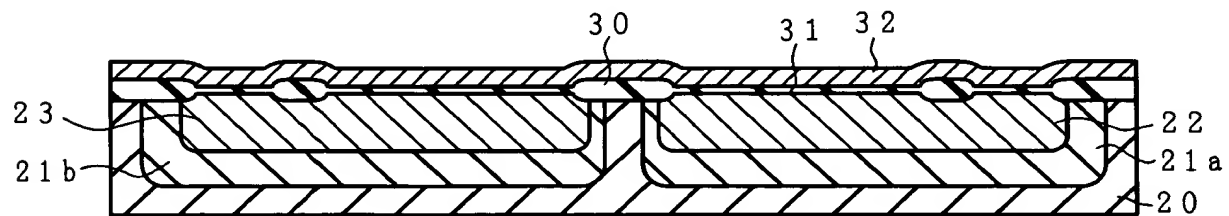
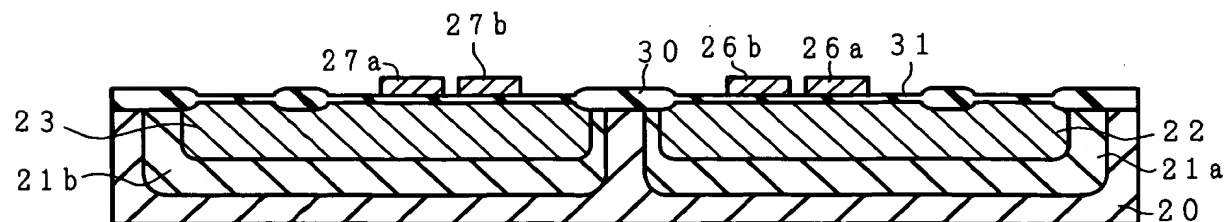


FIG. 10E



Sheet 10 of 16

FIG. 11A

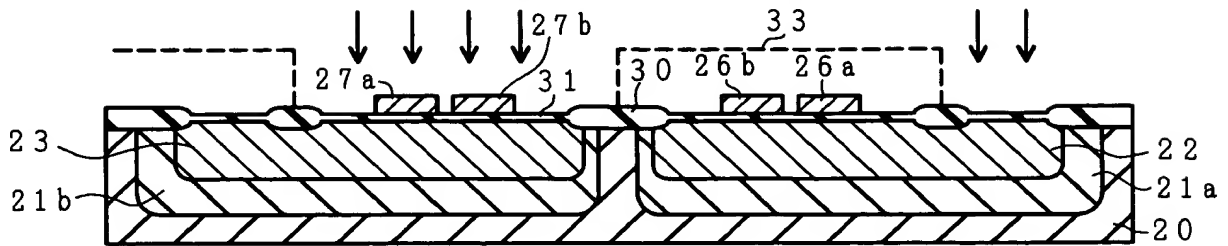


FIG. 11B

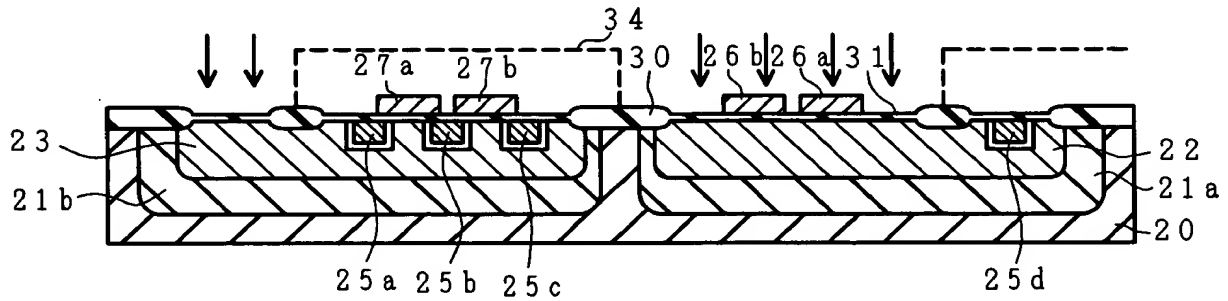


FIG. 11C

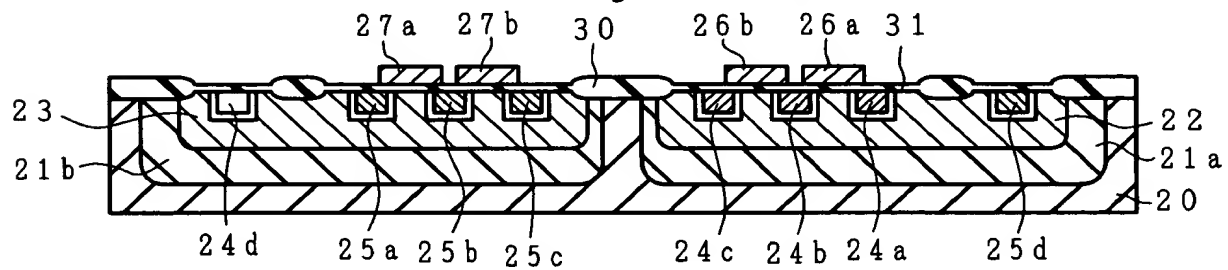


FIG. 11D

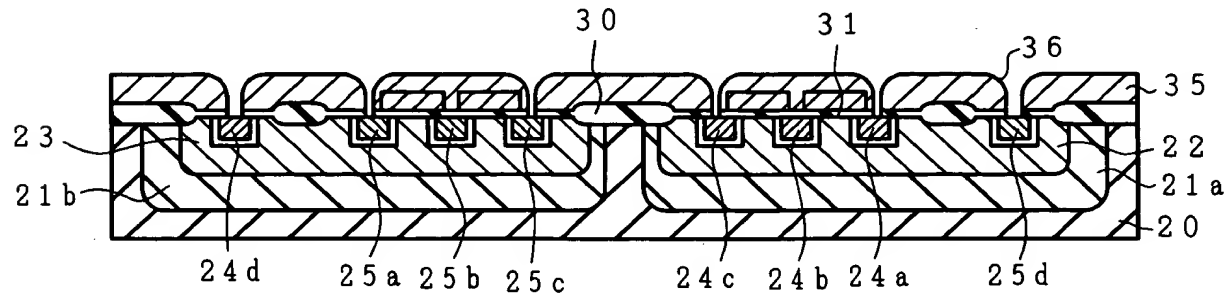
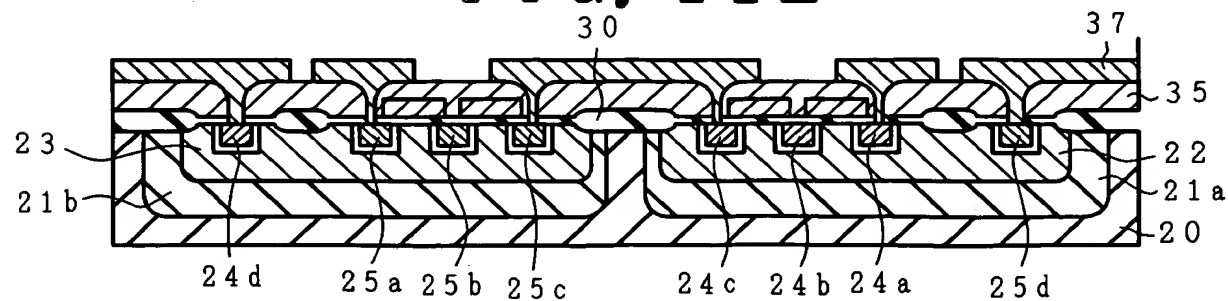


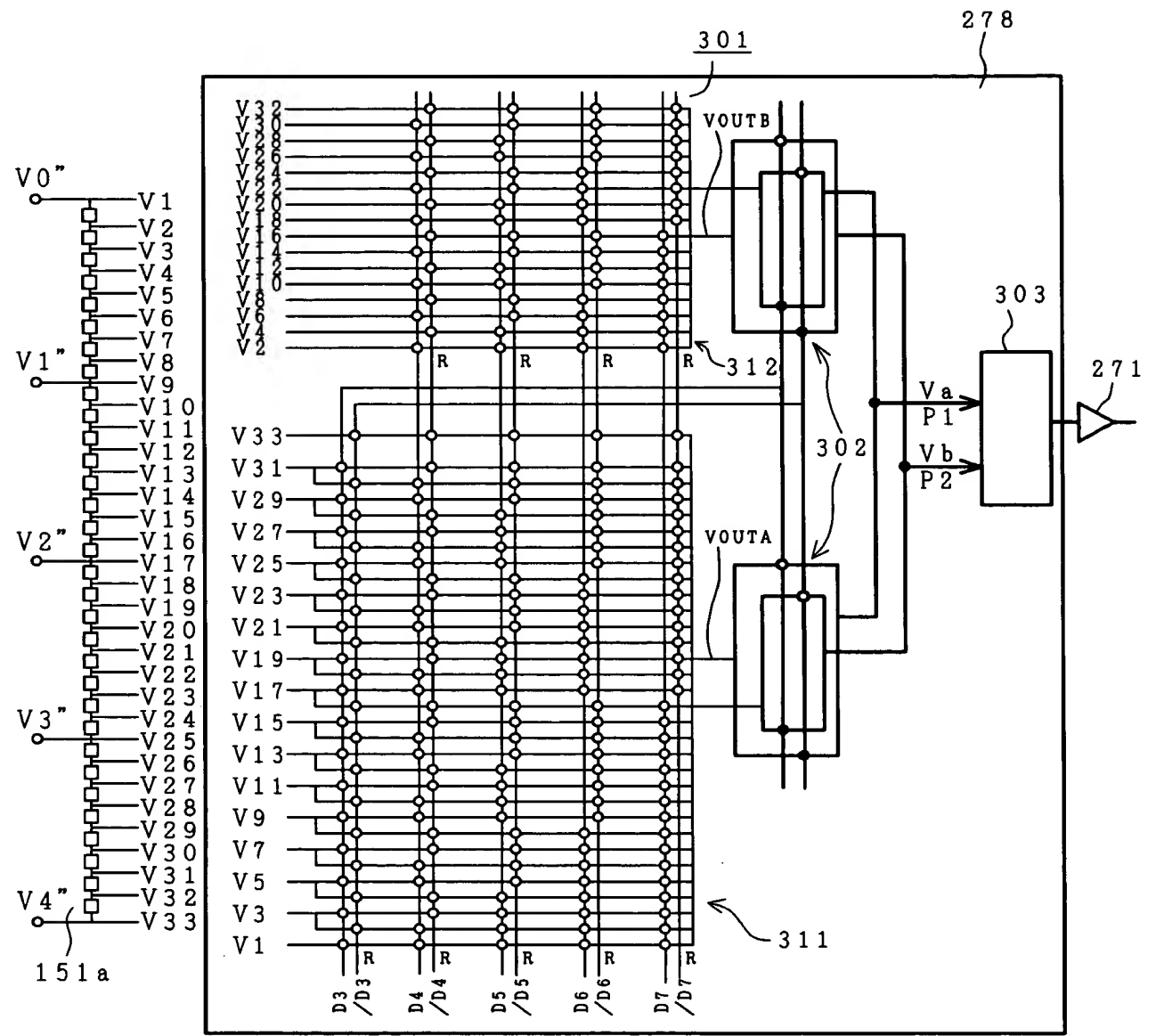
FIG. 11E



SECRET 28160

FIG. 12

SECRET



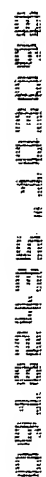


FIG. 14

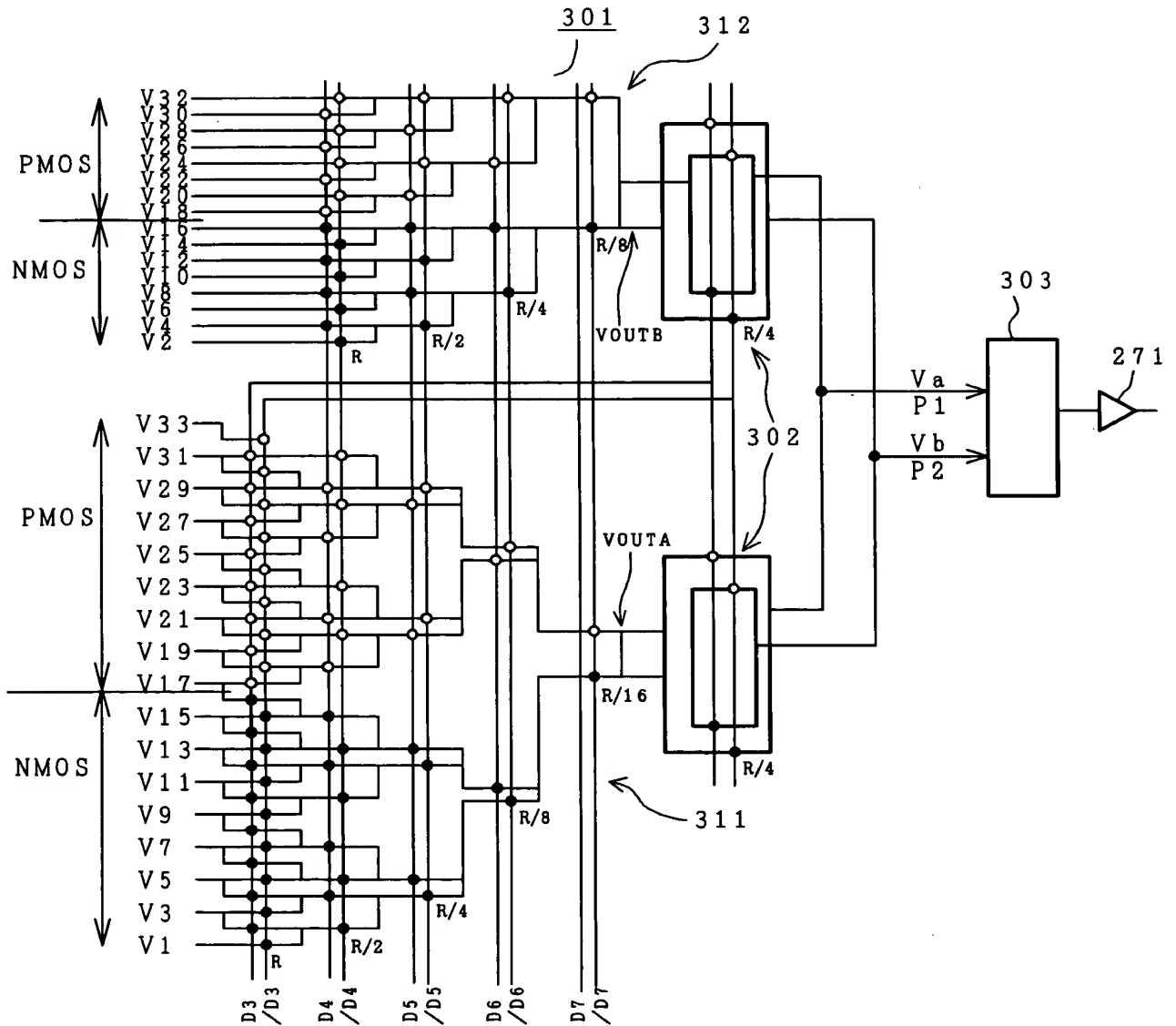
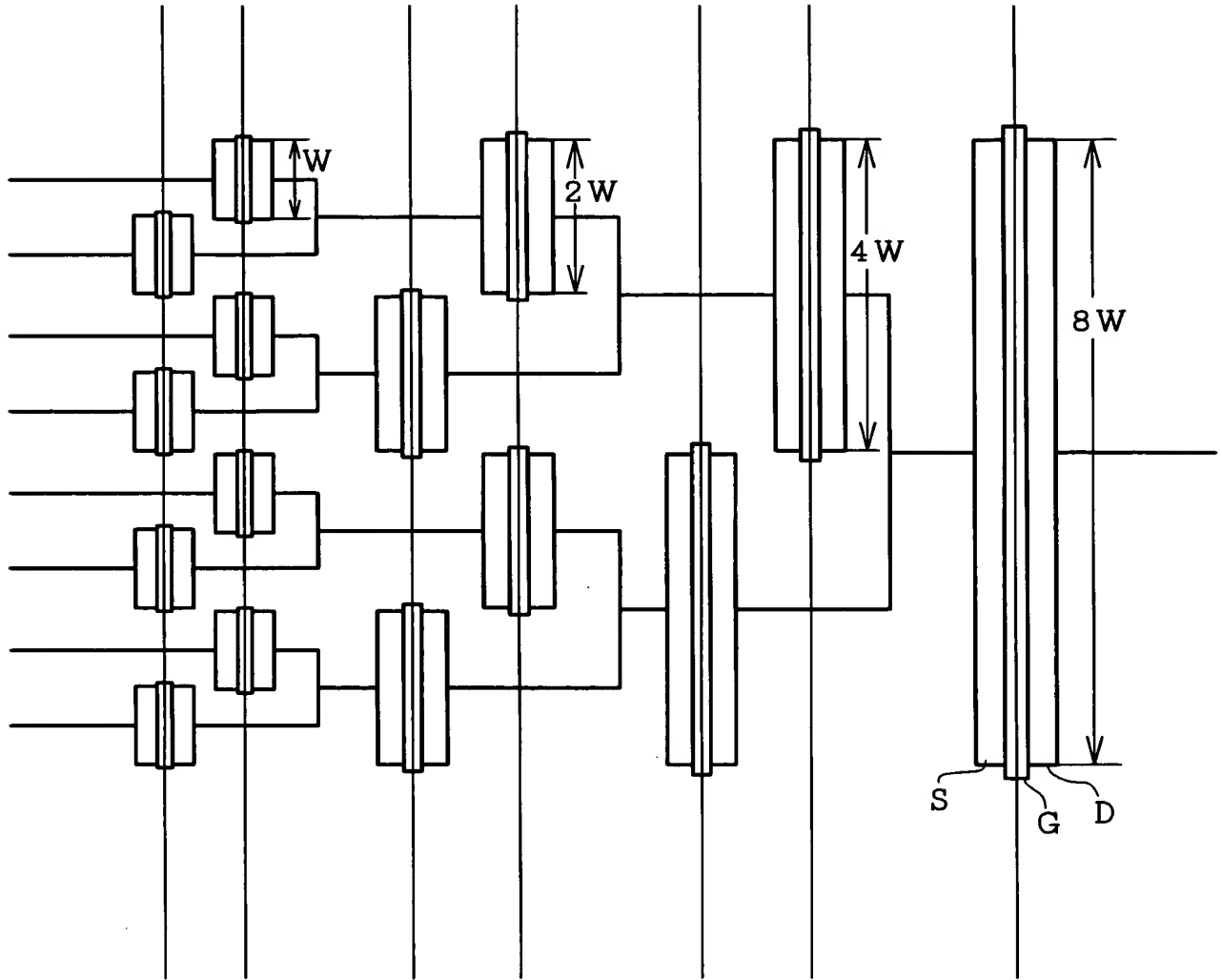
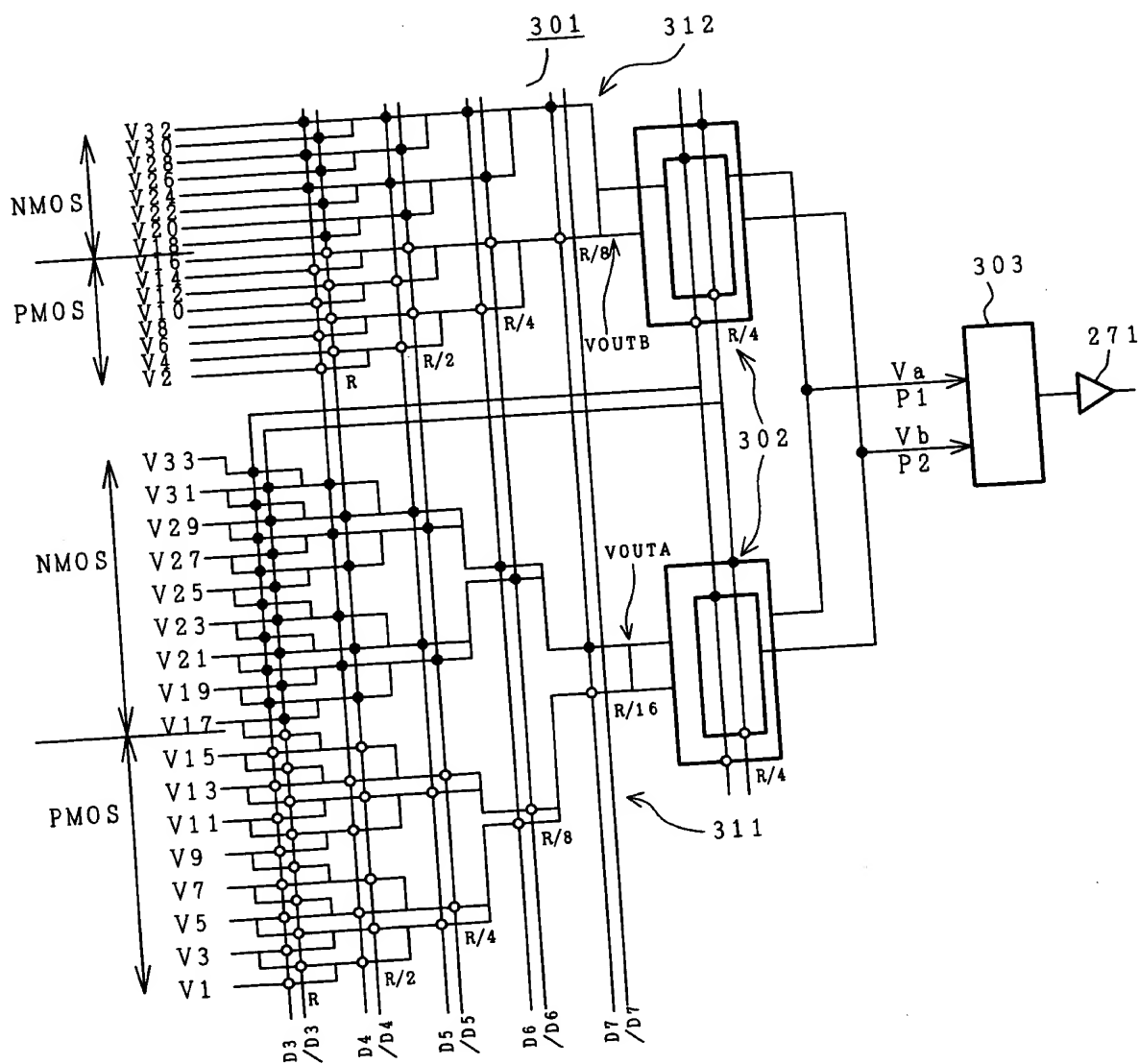


FIG. 15



SECRET 3423160

FIG. 16



200007-000000

FIG. 17

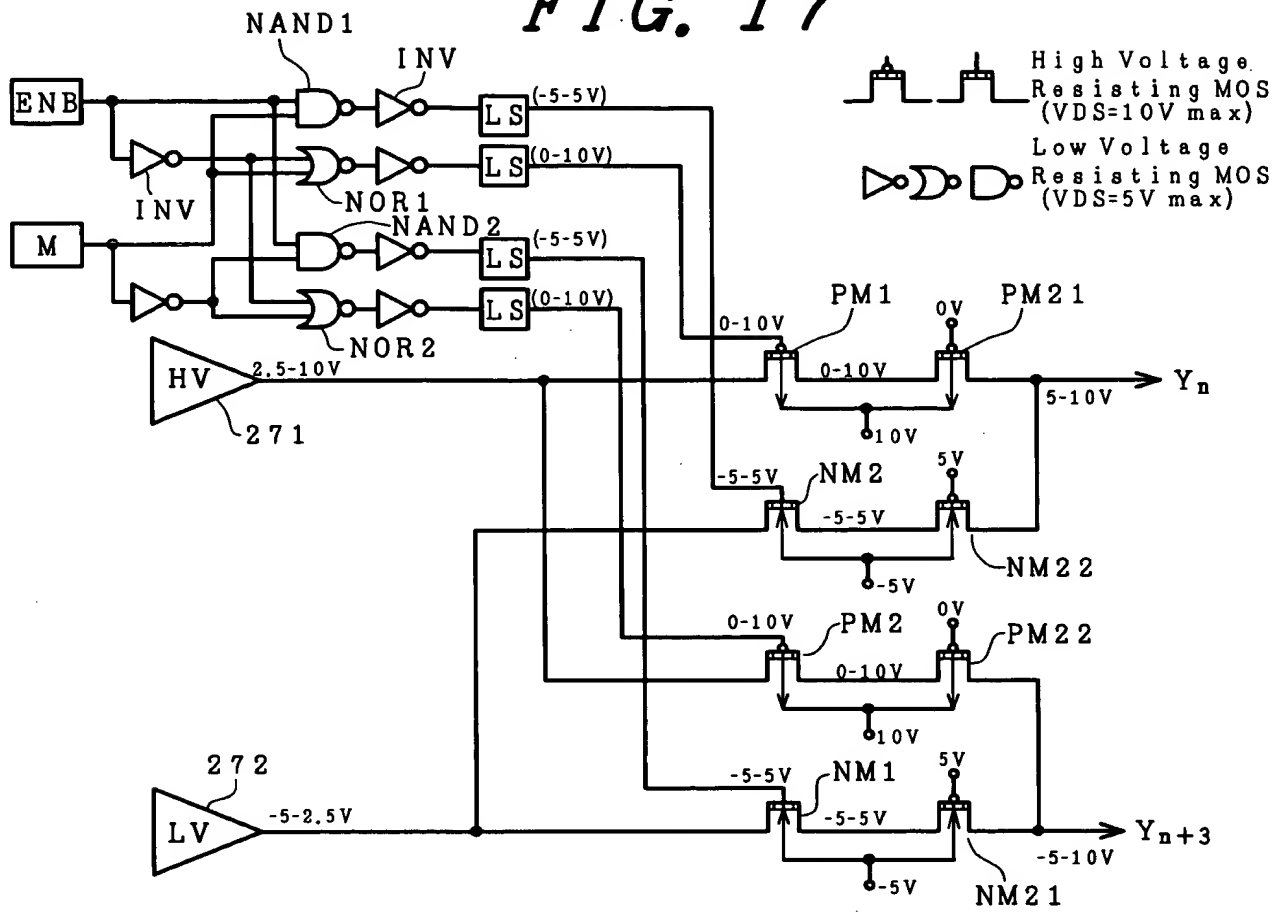
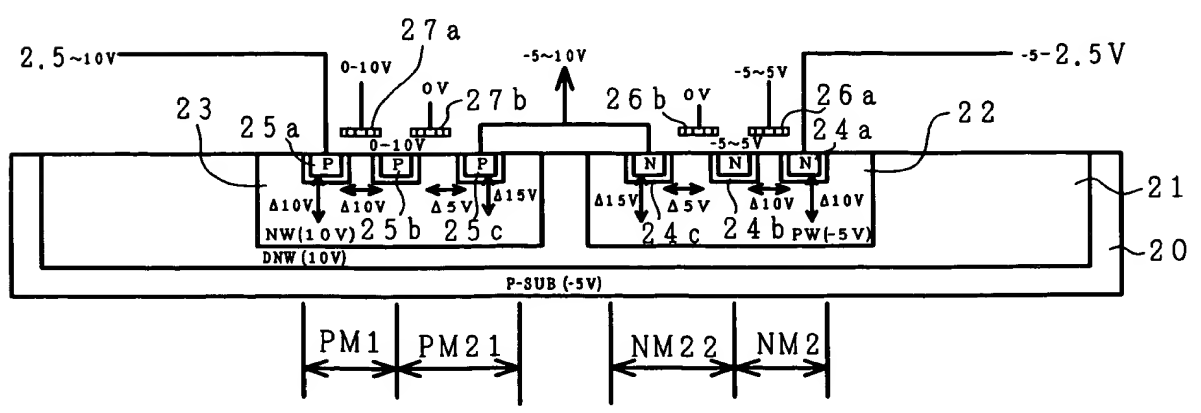


FIG. 18



SECRET 5428160

FIG. 19

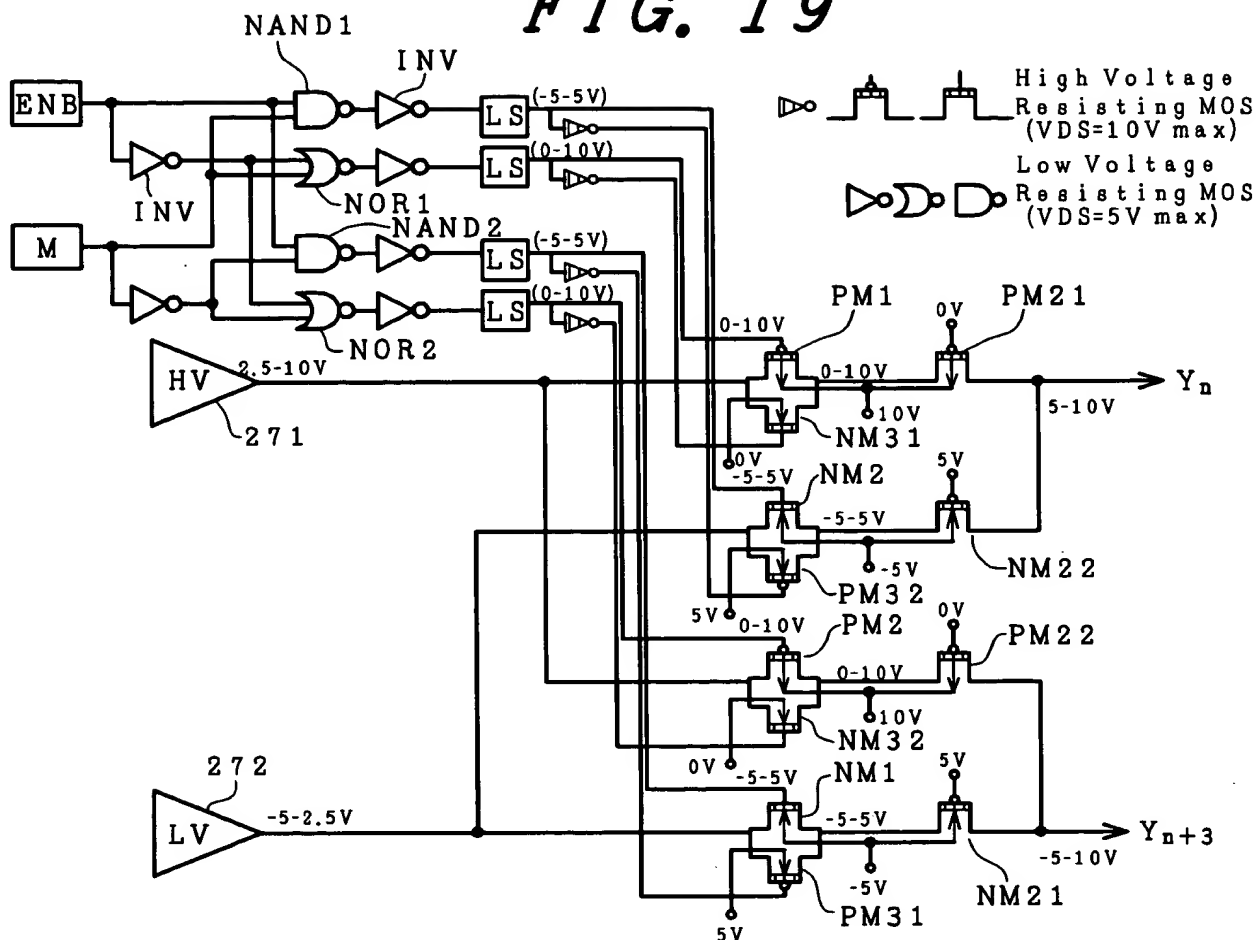


FIG. 20

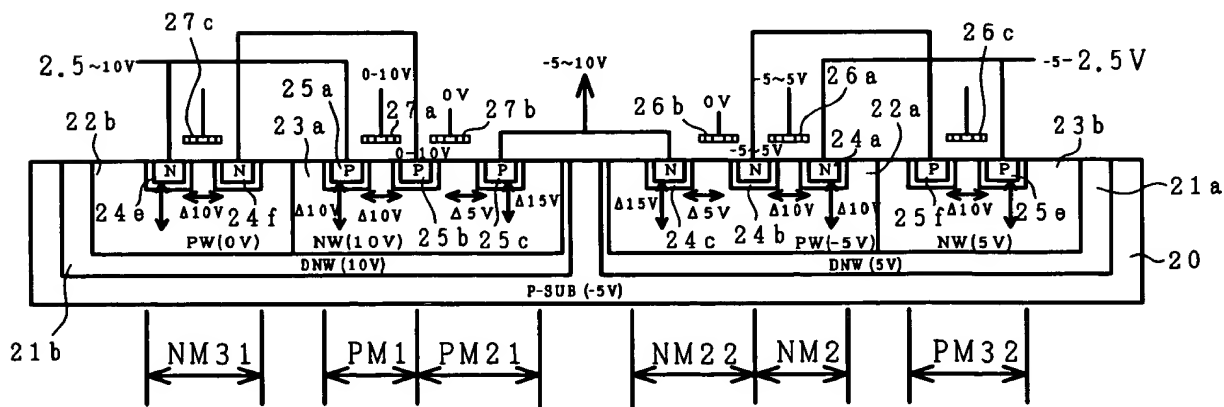


FIG. 22

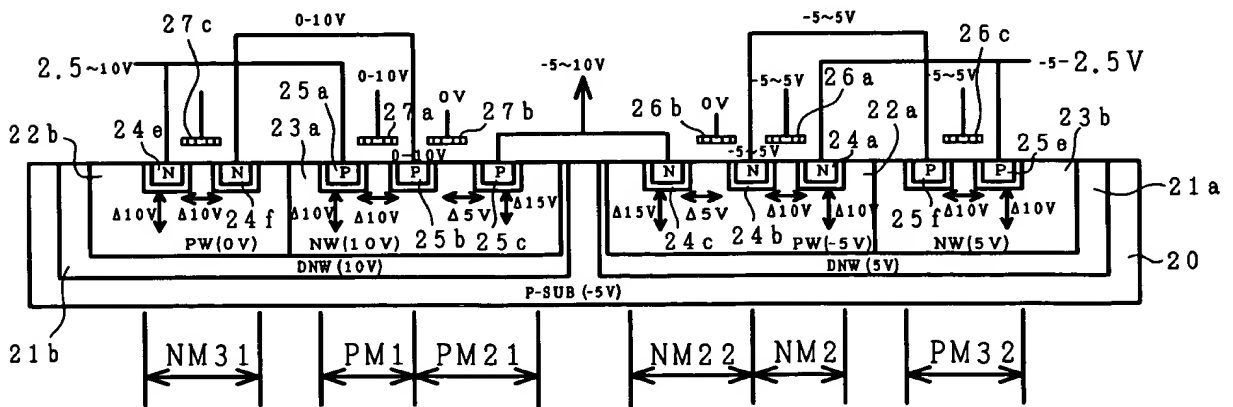


FIG. 23D

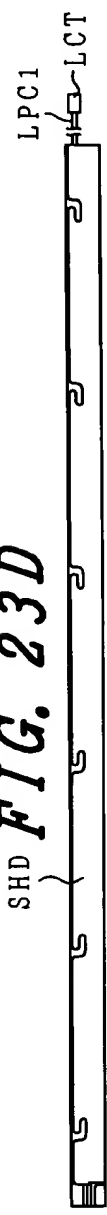


FIG. 23C

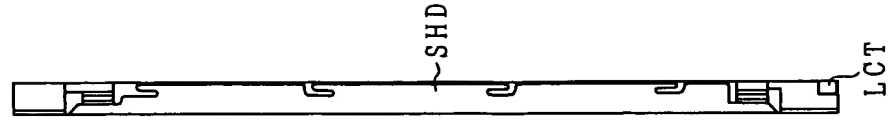


FIG. 23A

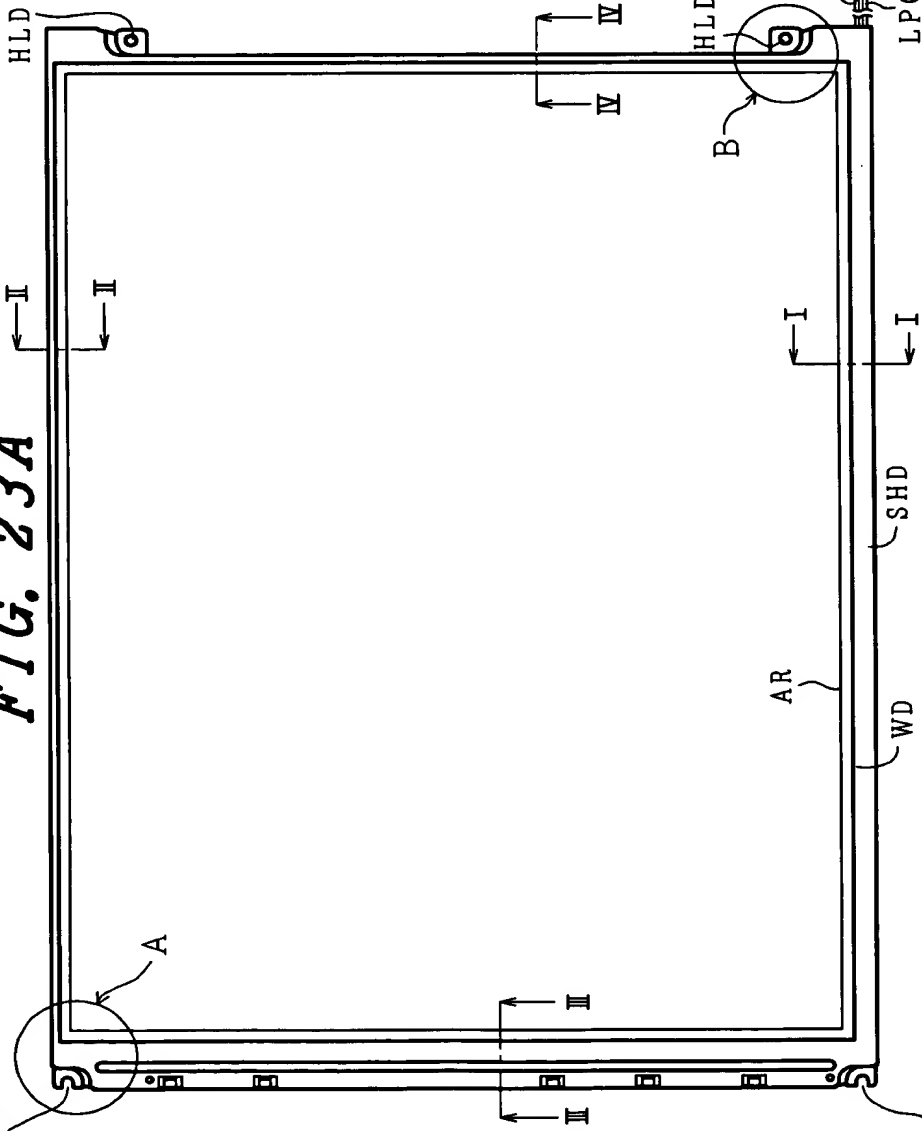


FIG. 23E



FIG. 23B

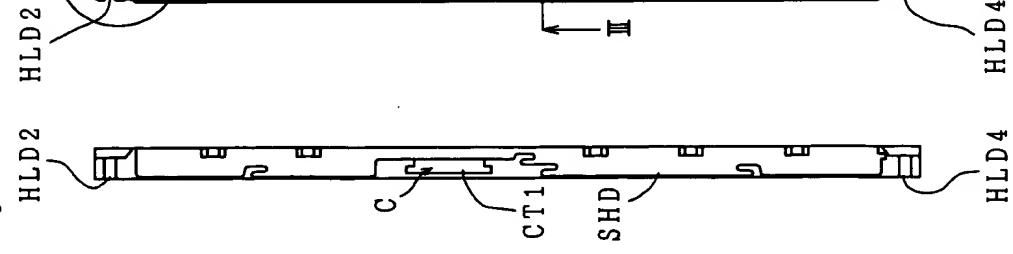
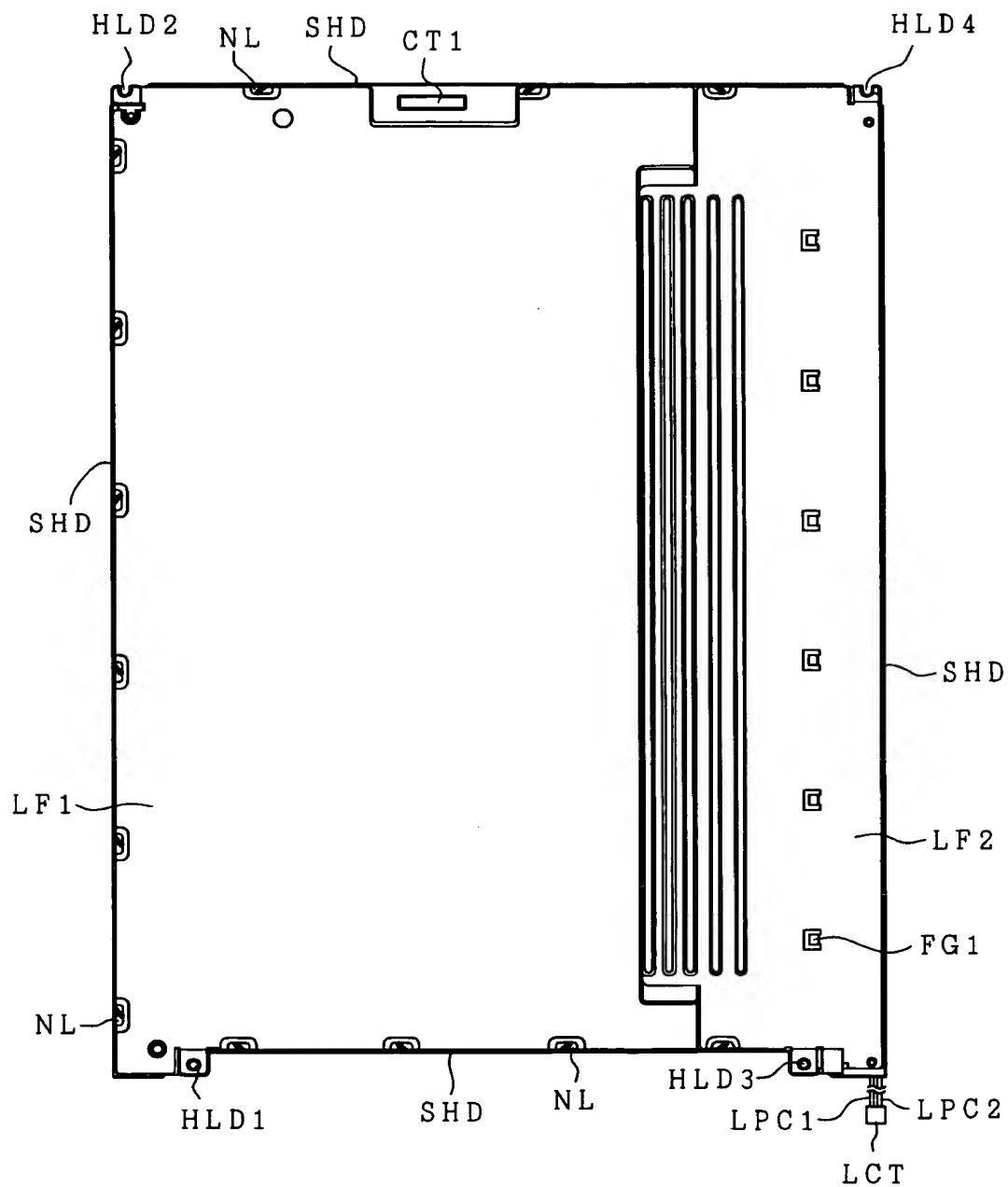


FIG. 24



0916435 103060

FIG. 25B

FIG. 25A

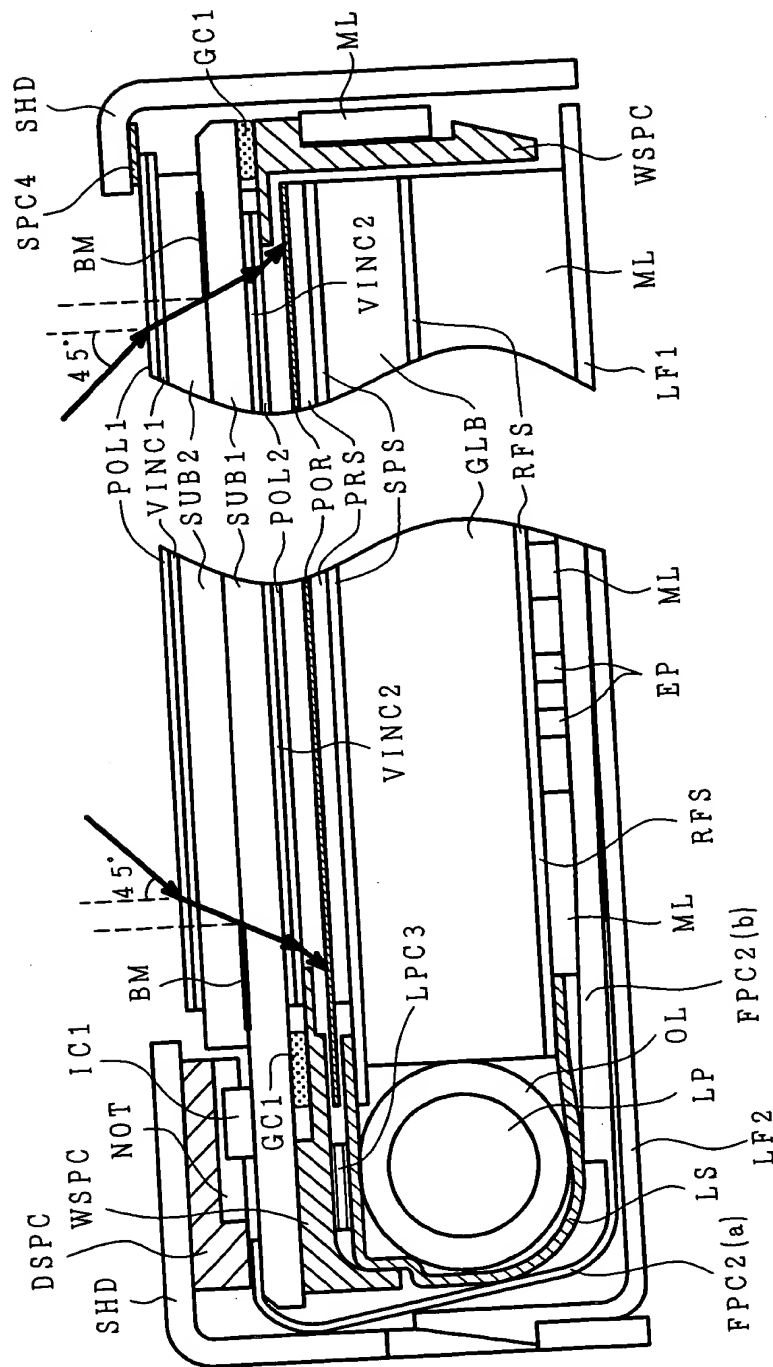
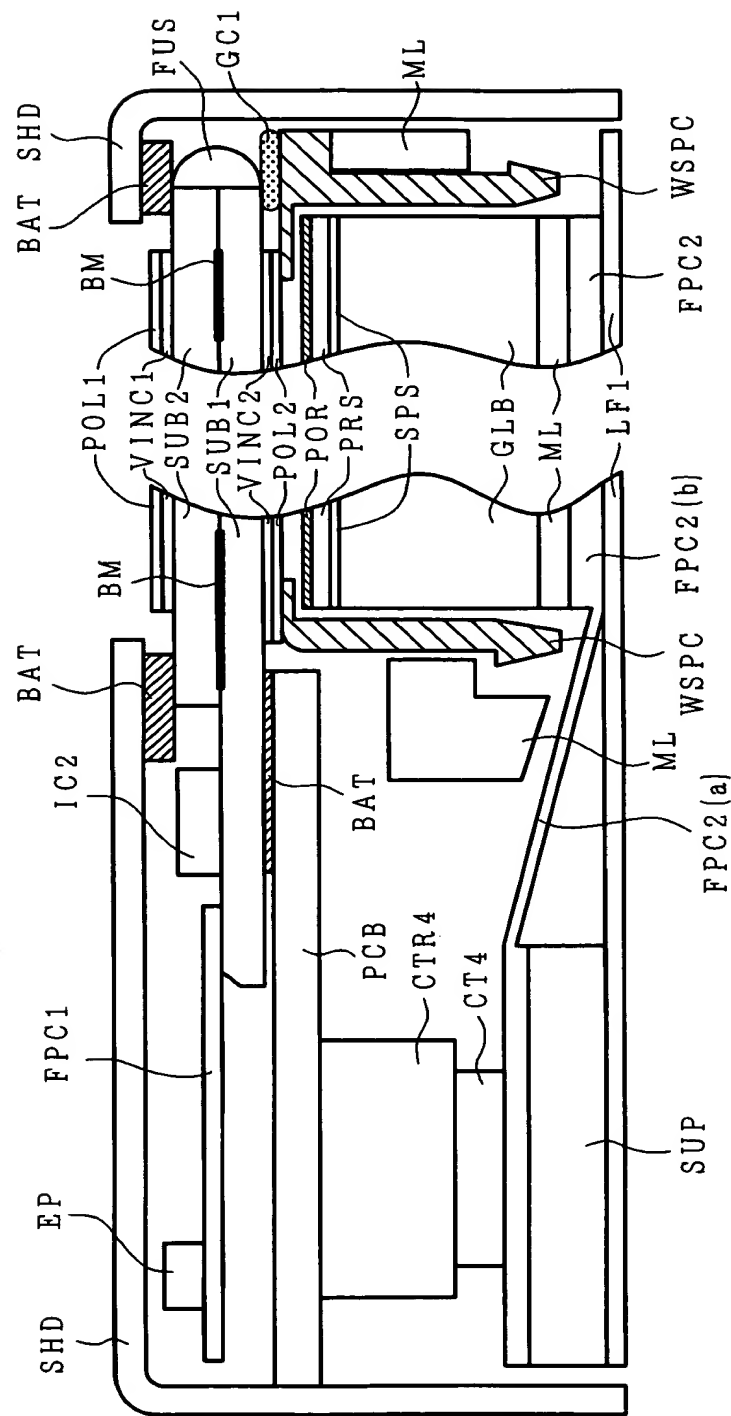


FIG. 26A

FIG. 26B



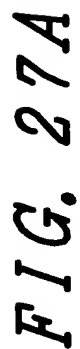


FIG. 27B

FIG. 28

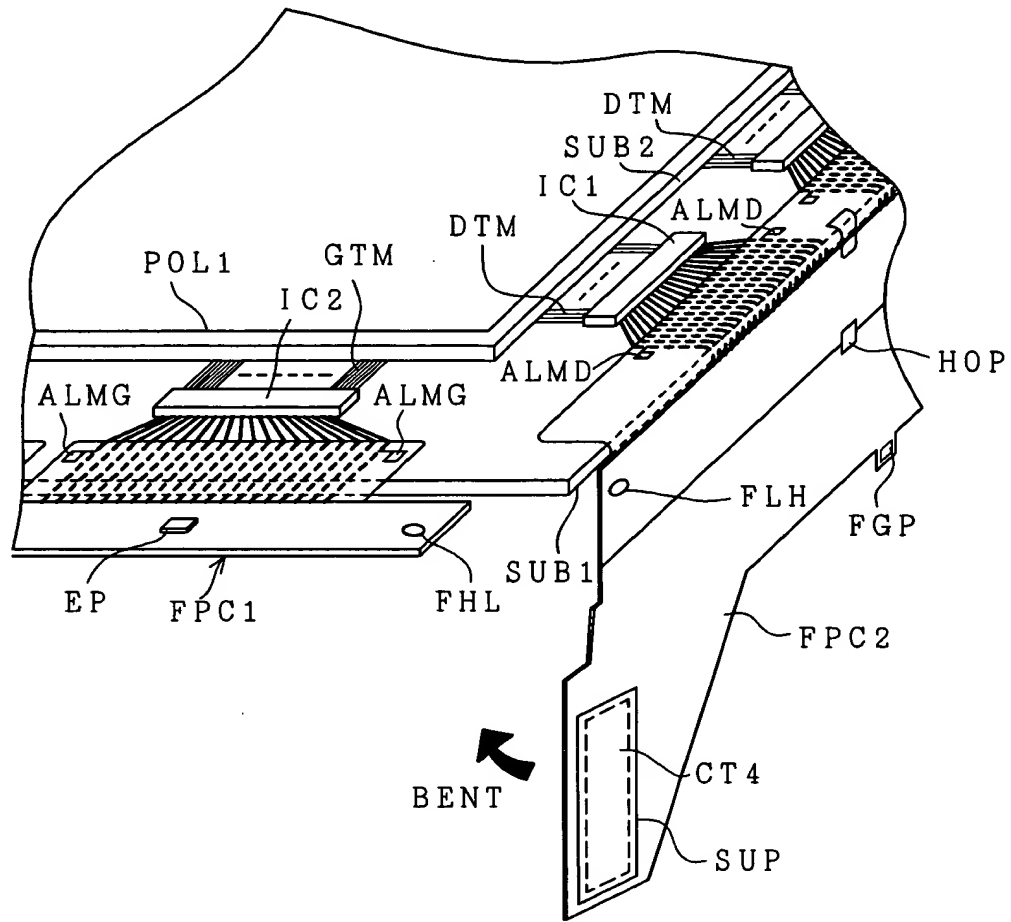


FIG. 29

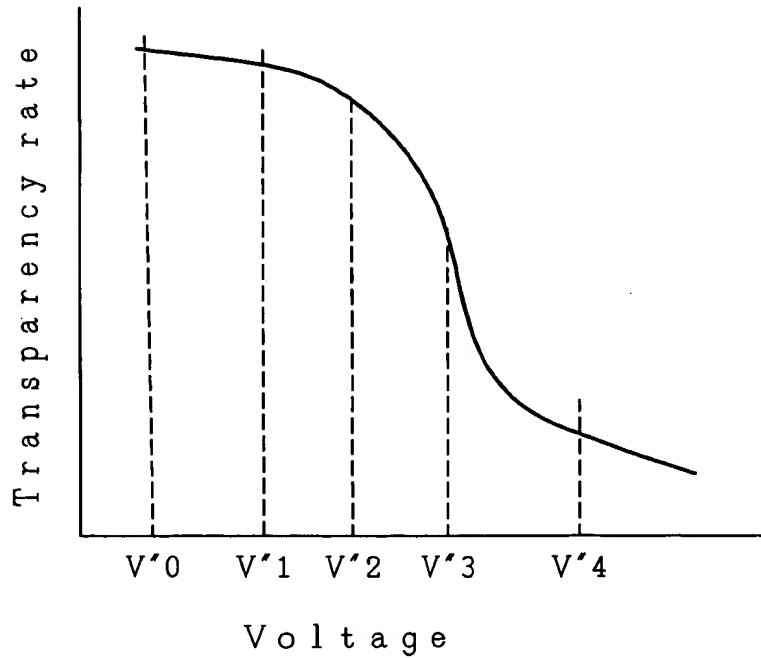


FIG. 30

